Update on bump bonding and (thin) pixel detector assemblies at CERN

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I would like to review:

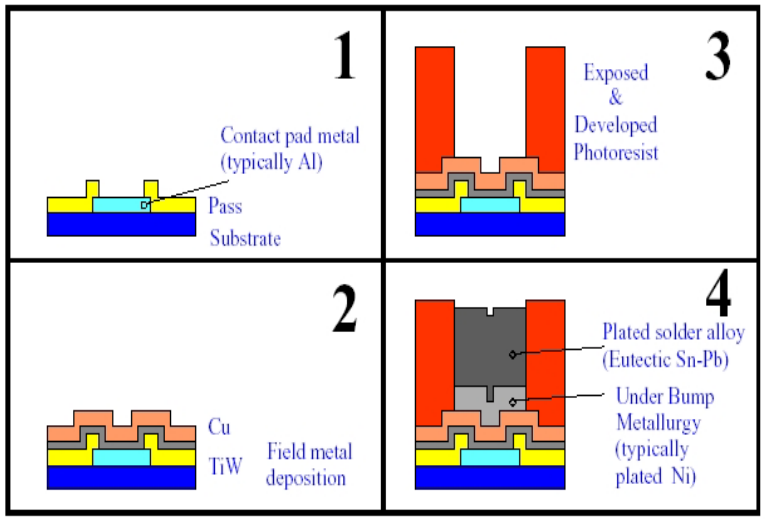
1.) Vendor of choice at CERN: VTT, Helsinki, for their integrated package of bump-bond deposition, wafer thinning and flip-chip bonding:

   a) - solder bump deposition on readout wafers,
      - solder beds on detector wafers
   b) optional thinning of readout wafers
   c) wafer dicing
   d) flip-chip bonding, 8” capability

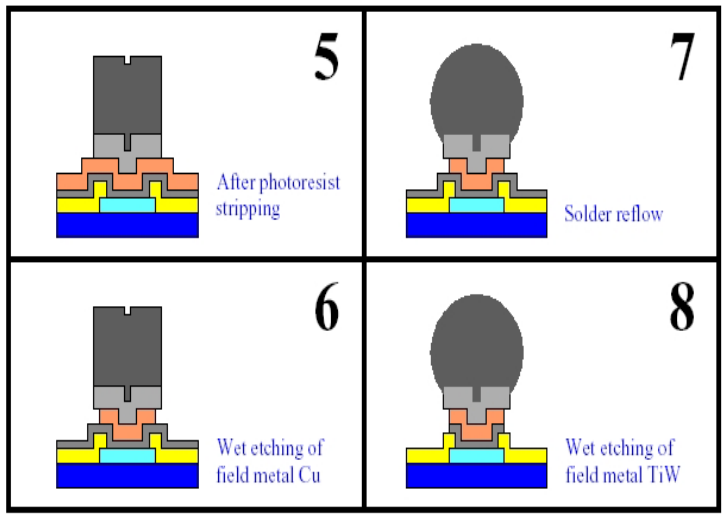
2.) Some results from recent NA60 and ALICE production.

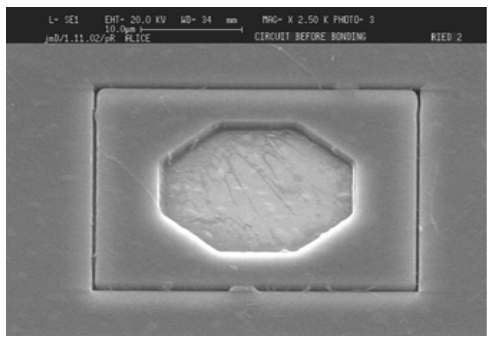
Bump bond deposition process

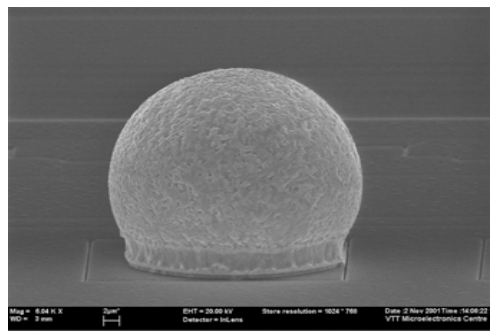
Bumping Process



Bumping Process [cont'd]

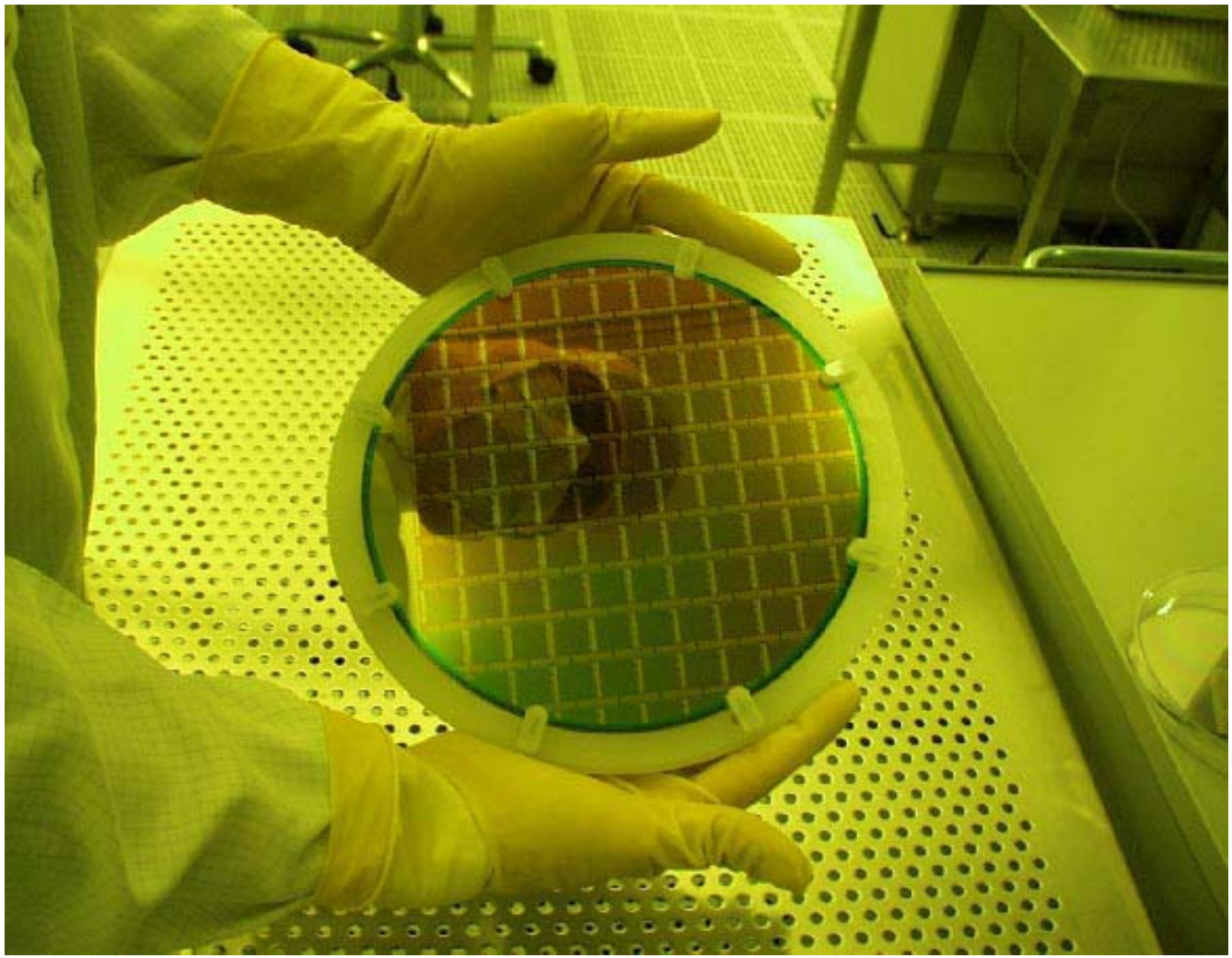






from step 1 → **to step 8**

Processing of 8'' ALICE1LHCb wafers at VTT



Flip Chip Bonding

Flip chip assembly is done in a Class-10 clean room.

Suss MicroTec FC150 Flip Chip Bonder with both Universal and Solder Reflow Bonding Arms.

PROCESS STEPS

① Preliminary alignment.
② Detector and readout chips are adjusted exactly parallel using a laser autocollimator.
③ Lateral alignment (x,y, θ).
④ Pre-bonding compression of softened bumps.
⑤ Reflow bonding.
⑥ Cooling.

NOTES

- Chips are heated through custom SiC vacuum tools using infrared halogen lamps.
- Alignment accuracy: < 3 μm.
- Throughput: 3-4 bondings/hour.

VTT is providing high-quality bump-bonding and flip-chip assembly. Problems that occurred in the second half of 2002 (leak in sputtering machine ⇒ loss of NA60 material) and spring 2003 (defective flip-chip bonder) have been solved.

Delivery of flip-chip assemblies to date:

- ALICE:
  - a few tens thick singles
  - a few thin singles
  - a few thick ladders
  - a few thin ladders

- NA60:
  - to date: 59 thick singles,
    45 (75% yield), 4 (0% yield), 10 (100%) yield.
  - being tested at CERN: 30 thick assemblies
  - in production: final 50 assemblies

Currently, the ongoing production for the completion of the NA60 pixel telescope has priority at VTT. To be finished in July. Then production of ALICE thin ladders resumes with priority.

NA60 assemblies: thick singles, 300µm sensor + 750µm chip

Typical high-quality assembly:

Test pulse measurement:

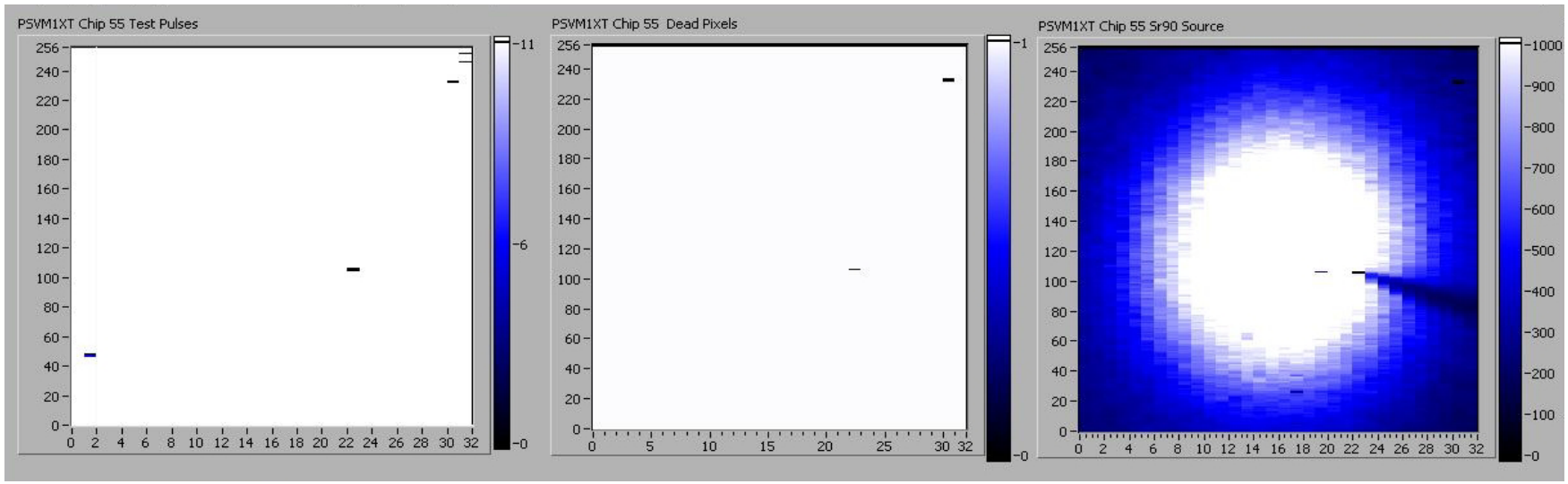
R/o chip: 8 of 8192 pixels dead. Rest of array OK.

Source measurement:

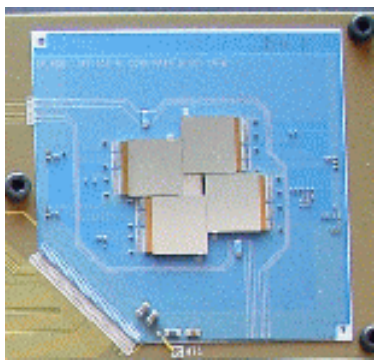
Bump bonding: 3 of 8192 bonds open. Rest of array OK.

Source measurement:

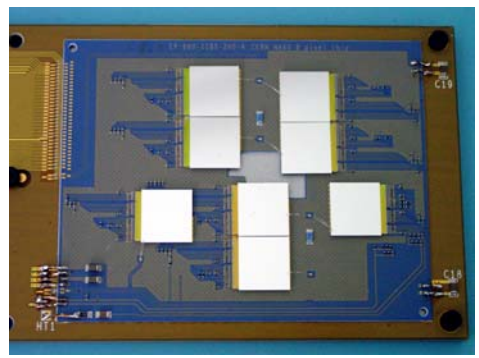
Image of Sr^{90} source with shadow of depletion voltage contact needle.



Used for construction of “4-chip” …



… and “8-chip” planes .



Wafer Thinning

Thinning is preferably done after bumping!

PROCESS STEPS

① Front side protection/planarization: UV-curable back grinding tape laminated on bumped wafer.

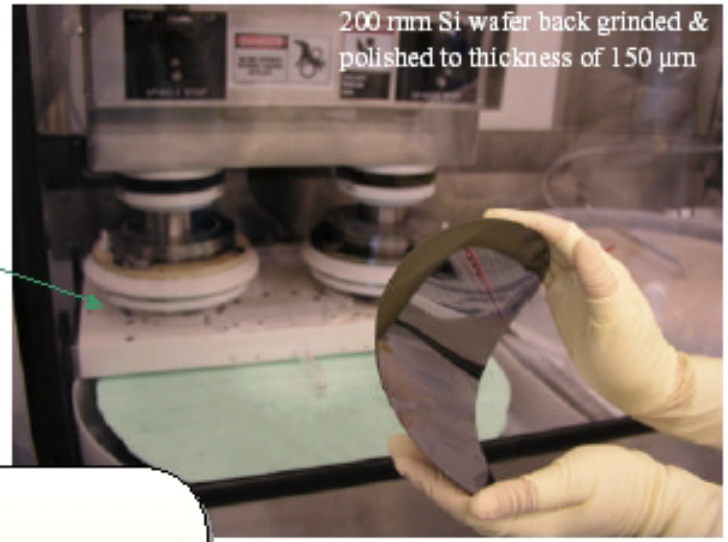
② Back grinding using diamond wheels with two different grit sizes (coarse + fine).

③ Defect layer left by mechanical grinding is removed by wet chemical etching or CMP (Chemical Mechanical Polishing).

④ Protective tape is UV-exposed and delaminated.

Strasbaugh 7AF Intelligent Grinder

Wafer Thinning [cont'd]

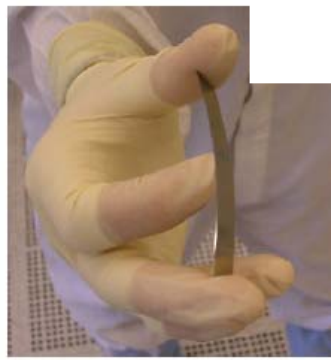


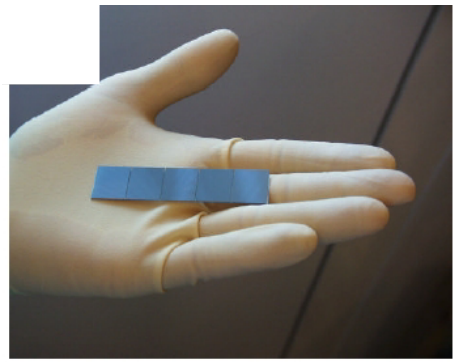
Strasbaugh 6DS-SP CMP System

NOTES

- Thickness down to 150 µm (200-mm/8" wafers).
- Total thickness variation (TTV) with protective tape < 5 µm over wafer.
- Post-grinding defect layer etching improves mechanical strength of die.

ALICE: thin ladder, i.e. 200µm sensor + 150µm readout chip





Idet @50V=180nA

Sr-Measurements :

	Chip43	Chip46	Chip42	Chip32	Chip30
Working pixels	99.7%	99.95%	99.98%	99.98%	100%
Missing pixels	28	4	2	2	0